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Substitute for form 1449/PTO				Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	10/630,537
				Filing Date	July 29, 2003
				First Named Inventor	Sandeep BHATIA
				Art Unit	2138
				Examiner Name	Phung M. CHUNG
Sheet	1	of	2	Attorney Docket Number	CA7034222001

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
PC	1	US- 6,079,040 A	06/20/2002	Hom et al.	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
PC	6	JP-2003-202362	07/18/2003	NEC Microsystems Ltd.		

Examiner Signature	/Phung Chung/	Date Considered	01/17/2007

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PA/52189327.1/2019535-7044222001

Substitute for form 1449B/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	Application Number	10/630,537
	Filing Date	July 29, 2003
	First Named Inventor	Sandeep BHATIA
	Art Unit	2138
	Examiner Name	Phung M. CHUNG

Sheet	2	of	2	Attorney Docket Number	CA7034222001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
PC	1	BALAKRISHNAN, K. J., et al., "Deterministic Test Vector Decompression in Software Using Linear Operations", Proceedings of the 21st IEEE VLSI Test Symposium, April 27 - May 1, 2003, pp. 225 - 231, IEEE, Los Alamitos, CA, USA.	
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PC	3	BHATIA, S., "Test Compaction by Using Linear-Matrix Driven Scan Chains", Proceedings of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, November 3 - 5, 2003, pp. 185 - 190, IEEE, USA.	
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PC	6	HSU, F. F. et al., "A Case Study on the Implementation of the Illinois Scan Architecture", Proceedings of the International Test Conference; 2001, pp. 538 - 547, International Test Conference, Washington, D.C., USA.	
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Examiner Signature	/Phung Chung/	Date Considered	01/17/2007

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